

Overview

This LSI is a single-chip microcontroller unit (MCU) built around the H8/300H CPU. Four I/O ports, ROM, RAM, EEPROM, a random number generator (RNG), a watchdog timer (WDT), a firewall management unit (FMU), interval timers (TMR1/TMR2), I²C bus interface (IIC2), synchronous serial communication unit (SSU), and a coprocessor are included.

Operating at a maximum 10-MHz internal clock rate, the H8/300H CPU rapidly executes bit manipulation instructions, arithmetic and logic instructions, and data transfer instructions.

The on-chip coprocessor executes modular multiplications (such as $ABR^{-1} \bmod N + kN$), which are used to calculate modular exponentiation $X^Y \bmod N$, and DES calculation processing at a high speed.

Table 1 lists the features of this LSI.

Table 1 Features

Item	Specification
CPU	H8/300H CPU Upper compatible with the H8/300 CPU in the object level Sixteen 16-bit registers (Sixteen 8-bit registers + eight 16-bit registers or Eight 32-bit registers) <ul style="list-style-type: none"> • High-speed operation <ul style="list-style-type: none"> — Maximum clock rate: internal clock 10 MHz — Add/subtract: 0.20 μs (10 MHz) — Multiply/divide: 1.40 μs (10 MHz) • Streamlined, concise instruction set <ul style="list-style-type: none"> — 16-bit variable instruction length: 2 to 10 bytes — arithmetic and logic operations between registers — MOV instruction for data transfer between registers and memory • Maximum 16-Mbyte address space • Instruction set features <ul style="list-style-type: none"> — 8-, 16-, or 32-bit transfer or arithmetic instructions — Unsigned or signed multiply instruction (8 bits \times 8 bits and 16 bits \times 16 bits) — Unsigned or signed divide instruction (16 bits \div 8 bits and 32 bits \div 16 bits) — Bit-accumulator instructions • Register-indirect specification of bit positions <ul style="list-style-type: none"> — EEPROM write instruction (EEPMOV.B instruction) — High-speed block transfer instruction (EEPMOV.W instruction)
I/O ports	<ul style="list-style-type: none"> • Four general-purpose input/output ports (Also used for interrupts) Note: When writing to the DDR7 to DDR4 bits, use the MOV instruction instead of the bit manipulation instruction.

Item	Specification
On-chip memory	<ul style="list-style-type: none"> • EEPROM: 16 kbytes + 2 kbytes (64 bytes × (256 + 32) pages) <ul style="list-style-type: none"> — Writing function by dedicated transfer instruction from CPU — Page write (1 byte to 64 bytes) and erase — Protected against accidental writing and erasing — Generates an EWE interrupt before an EEPMOV.B instruction is executed — On-chip high voltage generation circuit for writing and erasing — Built-in oscillator and timer — Write/erase time (maximum value): 3 ms (rewrite), 1.5 ms (erase) — Rewrite endurance: 1×10^5 times (-20°C to +75°C) — Data retention time: 10 years • ROM: 112 kbytes • RAM: 4 kbytes
Random number generator (RNG)	<ul style="list-style-type: none"> • Generates 16-bit random numbers. • Interrupts can be generated on completion of random number generation. • One of four random number generation times can be selected.
Watchdog timer (WDT)	<ul style="list-style-type: none"> • Generates a UDF interrupt constantly at any interval. • Stops the on-chip functions when the halt flag is set. • One of four counter clock sources can be selected.
Firewall management unit (FMU)	<ul style="list-style-type: none"> • Monitors memory access address of the user application. • Monitoring function of access between memory (monitors program execution on RAM and EEPROM)
Interval timer (TMR1/TMR2)	<ul style="list-style-type: none"> • Generates an interval interrupt constantly at any interval. • One of four counter clock sources can be selected. • Countable at a maximum of 4.5 seconds.
Modular multiplication coprocessor	<ul style="list-style-type: none"> • Modular multiplication ($ABR^{-1} \bmod N + kN$, etc.) • Modular exponentiation ($X^Y \bmod N$) with CPU control • Programmable data length: 160, 192, 256, 320, 384, 448, 512, 576, 640, 768, 896, or 1024 bits • Four operations: <ul style="list-style-type: none"> — Three types of modular multiplications: $ABR^{-1} \bmod N + kN$, $A^2R^{-1} \bmod N + kN$, and $AR^{-1} \bmod N + kN$ — One type of multiplication: $A \times N$ (A is fixed to 32 bits, and the maximum data length of operation results is 1024 bits) • 512-byte special-purpose registers <ul style="list-style-type: none"> — Four 128-byte (1024-bit) registers (Registers A, B, N, and W) — Can be used as RAM for the CPU when coprocessor calculations are not being performed • Interrupt request to the CPU when the coprocessor completes calculation • Built-in multiplier allows up to 4× speed operation.
Interrupt	<ul style="list-style-type: none"> • Four external interrupt pins: P1/\overline{IRQ} to P4/\overline{IRQ} <ul style="list-style-type: none"> — Used for interrupt input in sleep modes 1 and 2 — Same exception handling vector is assigned to the four pins • Internal interrupts (excluding TRAPA instruction) <ul style="list-style-type: none"> — Ten interrupt sources: EWE, UDF, RNG, TMR1, TMR2, IIC2, SSU, modular multiplication coprocessor, voltage monitor circuit, and clock multiplier <p>Notes: 1. When using I/O ports and sleep mode 1 is entered, clear DDR to 0 to use the pins as I/O input port pins before executing the SLEEP instruction. 2. Execute MOV instruction instead of bit manipulation when writing to bits DDR7 to DDR4. 3. Set the corresponding bit of IOIRQS to 1 when using the external interrupt on returning from sleep modes 1 and 2.</p>

Item	Specification
Security	<ul style="list-style-type: none"> • High frequency detector • High voltage detector • High temperature detector • Low frequency detector • Low voltage detector • Low temperature detector • Illegal access detector • Illegal instruction detector • EWE interrupt • RNG failure detector
Power-down states	Sleep modes 1 and 2 (sleep mode is entered by the SLEEP instruction)
Power-on reset circuit	<ul style="list-style-type: none"> • On-chip
On-chip oscillator	<ul style="list-style-type: none"> • Internal clock • CPU: 6 MHz ($\pm 20\%$) • Modular multiplication coprocessor: 12 MHz ($\pm 20\%$)
Power	<ul style="list-style-type: none"> • Single-voltage power supply 1.8 V to 3.6 V
Operating frequency range	<ul style="list-style-type: none"> • When the internal clock for the CPU is generated by dividing the external clock by 2 (CPUCS1, CPUCS0 = 00): $f_{CLK} = 1\text{ MHz to }8\text{ MHz}$ • When the external clock is directly supplied as the internal clock for the CPU (CPUCS1, CPUCS0 = 01): $f_{CLK} = 1\text{ MHz to }8\text{ MHz}$ • When the internal clock for the CPU is generated by multiplying the external clock by 1 by on-chip PLL (CPUCS1, CPUCS0 = 10): $f_{CLK} = 1\text{ MHz to }8\text{ MHz}$ • When the internal clock for the CPU is generated by multiplying the external clock by 2 by on-chip PLL (CPUCS1, CPUCS0 = 11): $f_{CLK} = 1\text{ MHz to }5\text{ MHz}$ <p>Operating frequency of the modular multiplication coprocessor is as follows:</p> <ul style="list-style-type: none"> • When 4\times speed calculation (PS1, PS0 = 10): $f_{COPRO} = 20\text{ MHz at maximum}$ • When 2\times speed calculation (PS1, PS0 = 01): $f_{COPRO} = 16\text{ MHz at maximum}$ • When 1\times speed calculation (PS1, PS0 = 00): $f_{COPRO} = 8\text{ MHz at maximum}$ (f_{CLK}: externally input clock frequency; f_{COPRO}: operating frequency of the modular multiplication coprocessor)
Operating temperature	<ul style="list-style-type: none"> • $-20\text{ to }+75^{\circ}\text{C}$
Other function	<ul style="list-style-type: none"> • Cold/Warm reset judgment function • System clock multiplying function by PLL circuit

Block Diagram

Figure 1 is a block diagram of this LSI.

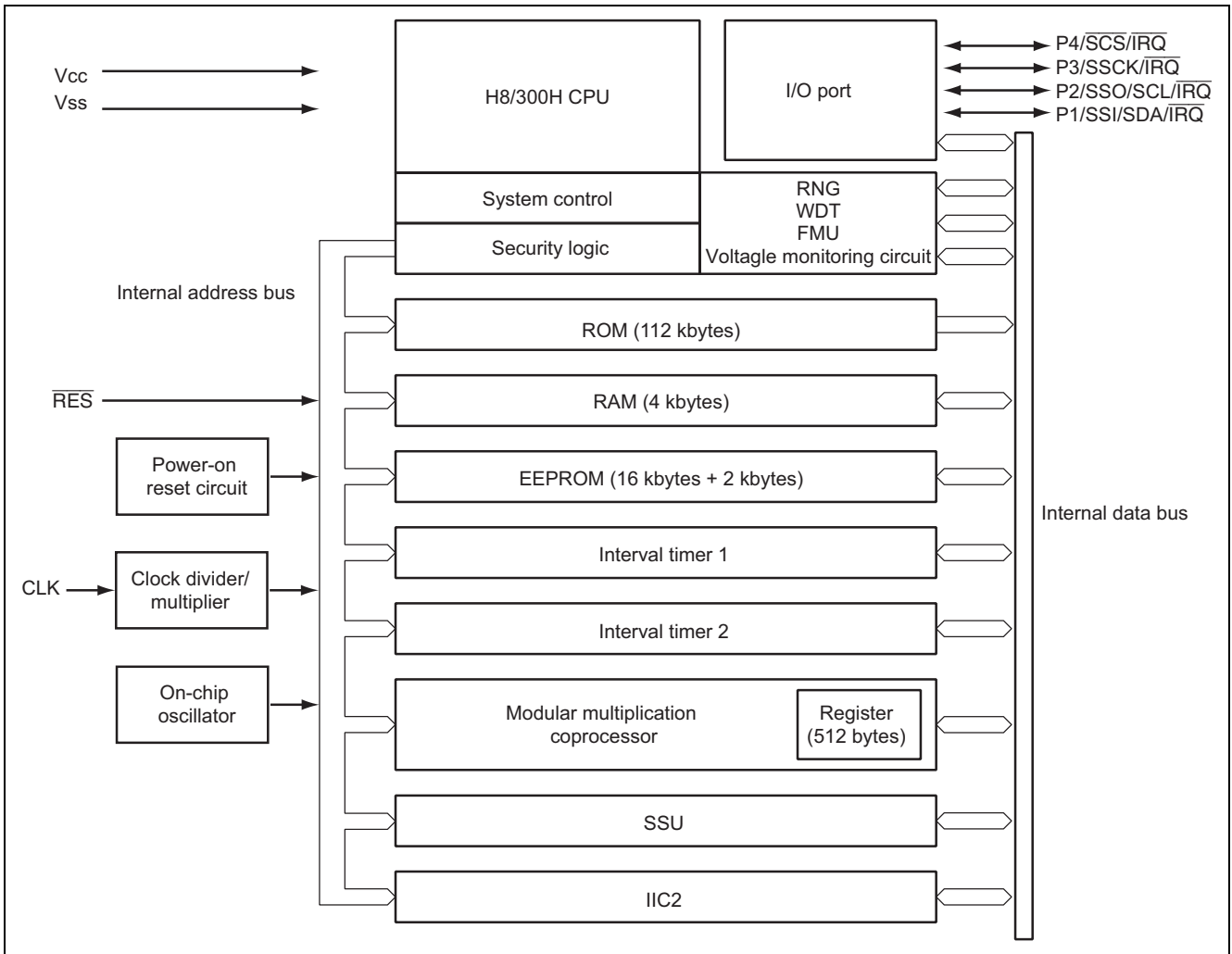


Figure 1 Block Diagram

Pin Assignment

Figure 2 shows the pin arrangement of this LSI.

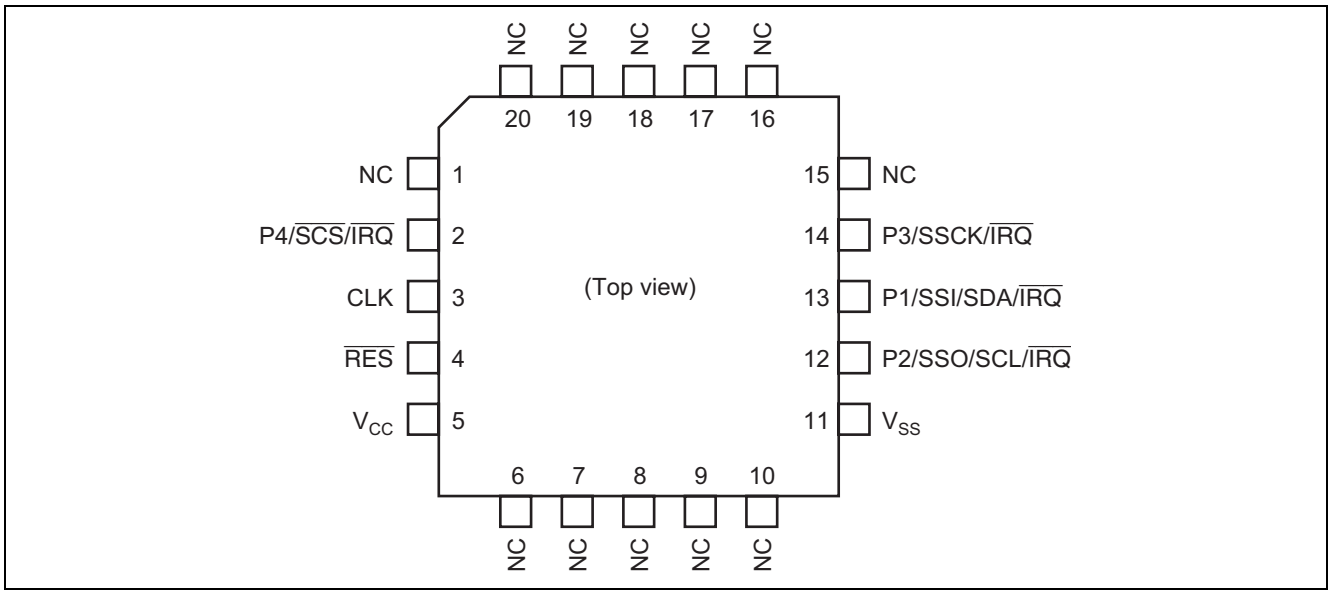


Figure 2 Pin Assignment

Pin Functions

Table 2 lists the pin functions of this LSI.

Table 2 Pin Functions

Type	Symbol	I/O	Name and Description
Power supply	V_{CC}	I	Power supply pin: 3.0 V to 3.6 V
	V_{SS}	I	Ground pin: 0 V
Clock	CLK	I	External clock input pin
Reset	\overline{RES}^{*1}	I	Reset pin: Low-level input resets the chip.
I ² C bus interface 2 (IIC2)	SCL	I/O	IIC2 clock input/output pin
	SDA	I/O	IIC2 data input/output pin
Synchronous serial communication unit(SSU)	SSI	I/O	SSU data input/output pin
	SSO	I/O	SSU data input/output pin
	SSCK	I/O	SSU clock input/output pin
	\overline{SCS}	I/O	SSU chip select input/output pin
External interrupt	\overline{IRQ}^{*2}	I	Interrupt pin: In sleep modes 1 and 2, this pin can be used as an interrupt input pin.
Port	P1	I/O	I/O port pin: Input or output can be selected by software.
	P2	I/O	I/O port pin: Input or output can be selected by software.
	P3	I/O	I/O port pin: Input or output can be selected by software.
	P4	I/O	I/O port pin: Input or output can be selected by software.

Notes: 1. An input pull-up MOS is connected to the \overline{RES} pin as shown in figure 3.

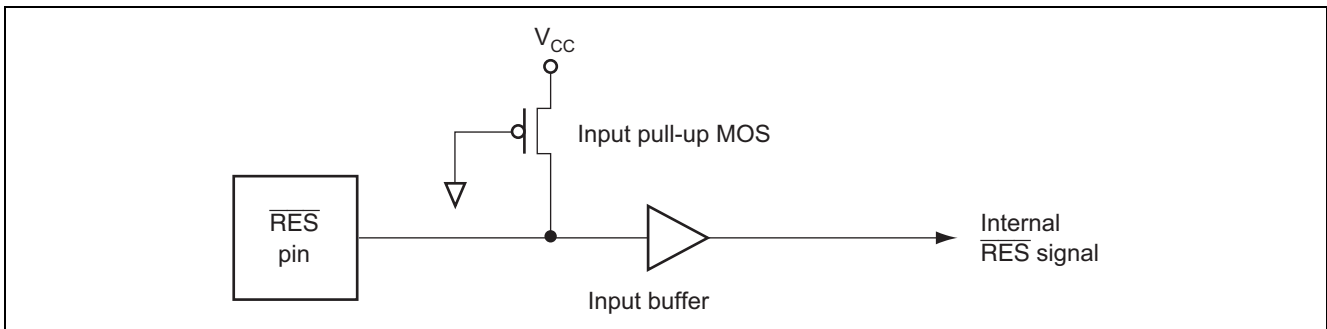


Figure 3 Block Diagram of the \overline{RES} Pin

2. The P1/ \overline{IRQ} to P4/ \overline{IRQ} pins can be used as data I/O and interrupt input pins. Input pull-up MOSs are connected to these pins.

Electrical Characteristics

Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{in}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature	T_{stg}	-55 to +75	°C

Note: Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the recommended operating conditions. Exceeding these conditions could affect the reliability of the chip.

DC Characteristics

Table 4 DC Characteristics

Conditions: $V_{CC} = 1.8$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise specified.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Input high voltage	$\overline{\text{RES}}$, CLK P1, P2, P3, P4 SDA, SCL, $\overline{\text{SCS}}$, SSCK, SSI, SSO	V_{IH}	$V_{CC} = 3.0$ to 3.6 V	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V
			$V_{CC} = 1.8$ to 3.0 V	$V_{CC} \times 0.85$	—	$V_{CC} + 0.3$	V
Input low voltage	$\overline{\text{RES}}$, CLK P1, P2, P3, P4 SDA, SCL, $\overline{\text{SCS}}$, SSCK, SSI, SSO	V_{IL}	$V_{CC} = 3.0$ to 3.6 V	-0.3	—	$V_{CC} \times 0.2$	V
			$V_{CC} = 1.8$ to 3.0 V	-0.3	—	0.2	V
Output high voltage	P1, P2, P3, P4 $\overline{\text{SCS}}$, SSCK, SSI, SSO	V_{OH}	$I_{OH} = -200$ μA	$V_{CC} \times 0.7$	—	V_{CC}	V
Output low voltage	P1, P2, P3, P4 SDA, SCL, $\overline{\text{SCS}}$, SSCK, SSI, SSO	V_{OL}	$I_{OL} = 1$ mA	0	—	0.4	V
Input leakage current	P1, P2, P3, P4, CLK	$ I_{in} $	$V_{in} = 0.5$ to $V_{CC} - 0.5$ V	—	—	10	μA
Input pull-up MOS current* ¹	$\overline{\text{RES}}$	$-I_p$	$V_{in} = 0$ V	—	—	150	μA
	P1, P2, P3, P4			—	—	150	μA
Supply Current* ²	CPU half of the external clock/ external clock	Coprocessor stops* ³	I_{CC}	—	—	7.5	mA
	CPU multiplied by one with PLL	Exclusive mode* ³		—	—	7.5	
	CPU multiplied by two with PLL	Normal speed of coprocessor in maximum mode* ³		—	—	10	
Supply Current* ²	Sleep mode 1		V_{in} (I/O ports and $\overline{\text{RES}}$) $= V_{CC} - 0.5$ V to V_{CC} or I/O ports open* ¹ $T_a \leq 50^\circ\text{C}$	—	—	100	μA
				V_{in} (I/O ports and $\overline{\text{RES}}$) $= V_{CC} - 0.5$ V to V_{CC} or I/O ports open* ¹ $T_a > 50^\circ\text{C}$	—	—	200
Pin capacitance		C_p	$V_{in} = 0$ V, $f_{CLK} = 1$ MHz, $T_a = 25^\circ\text{C}$	—	—	15	pF

- Notes: 1. The input pull-up MOS's in the $\overline{\text{RES}}$ is always turned on, even in sleep mode 1 and sleep mode 2. To avoid the input pull-up MOS current, the $\overline{\text{RES}}$ must be kept high during sleep mode 1 and sleep mode 2.
2. $V_{IHmin} = V_{CC} - 0.5$ V, $V_{ILmax} = 0.5$ V, and values are when all output pins are unloaded.
3. These are operating modes other than sleep mode 1. In this case, CLK must be input according to the DC and AC characteristics.

AC Characteristics

Table 5 AC Characteristics

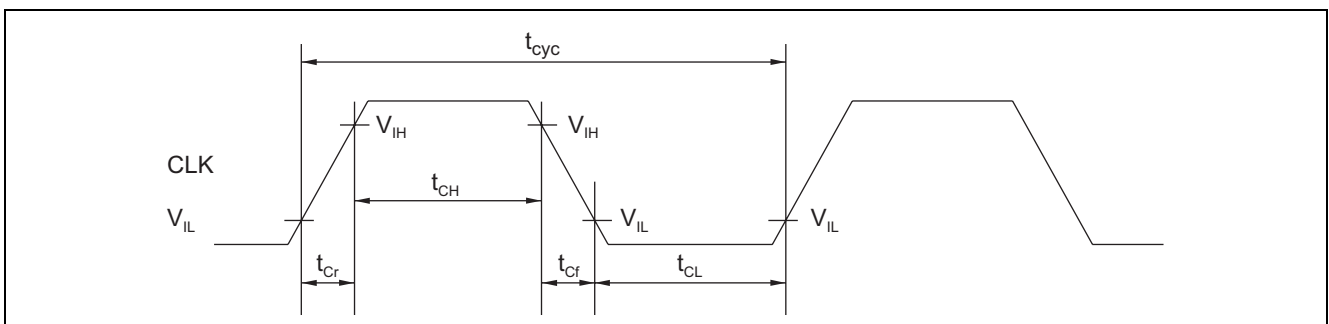
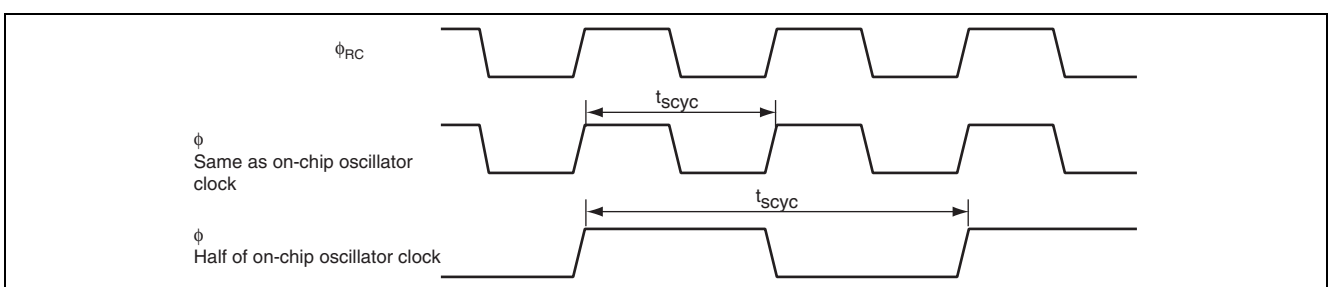
Conditions: $V_{CC} = 1.8$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise specified.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Clock cycle time (external clock)	t_{cyc}	Figure 4.1	See table 7				
System clock (ϕ) cycle time (Internal clock, CPUCS = 0)	t_{scyc}	Figure 4.2	278	333	417	ns	
System clock (ϕ) cycle time (Internal clock, CPUCS = 1)	t_{scyc}	Figure 4.2	139	166	208	ns	
System clock (ϕ) cycle time (External clock)	t_{scyc}	Figure 4.3	100	—	2000	ns	
Clock high-level width	t_{CH}	Figure 4.1	0.4	—	0.6	t_{cyc}	
Clock low-level width	t_{CL}	Figure 4.1	0.4	—	0.6	t_{cyc}	
Clock fall time	t_{Cf}	Figure 4.1	—	—	0.09*	t_{cyc}	
Clock rise time	t_{Cr}	Figure 4.1	—	—	0.09*	t_{cyc}	
I/O port input fall time	t_f	Figure 5	—	—	1.0	μs	
I/O port input rise time	t_r	Figure 5	—	—	1.0	μs	
RES pulse width	Cold reset	t_{RWL1}	Figure 6	500	—	—	μs
	Warm reset	t_{RWL2}	Figure 6	400	—	—	t_{scyc}
Power supply ON time	t_{ON}	Figure 6	0	—	—	ms	
Power supply OFF time	t_{OFF}	Figure 6	0	—	—	ms	
EEPROM write time		Rewrite		—	—	3	ms
		Erase		—	—	1.5	ms
Clock hold time	t_{CLKH}	Figure 7	400	—	—	t_{cyc}	
Clock setup time	t_{CLKS}	Figure 7	20	—	—	t_{cyc}	
Interrupt pulse width (IRQ)	Sleep mode 2	t_{IRQW}	Figure 7	4	—	—	t_{scyc}
	Other modes			400	—	—	ns

Notes: * Set CLK so as no noise is generated by the clock input and the frequency of the clock signal increases or decreases monotonically.

Table 6 Clock Cycle TimesConditions: $V_{CC} = 1.8$ to 3.6 V, unless otherwise specified.

Item	Coprocessor Operation	Min.	Typ.	Max.	Unit
CPU is driven by an external clock divided by 2	Stopped or normal speed operation ($V_{CC} = 1.8$ to 3.0 V)	0.2	—	1.0	μ s
	Stopped or normal speed operation ($V_{CC} = 3.0$ to 3.6 V)	0.125	—	1.0	μ s
	Double speed operation ($V_{CC} = 1.8$ to 3.0 V)	0.2	—	1.0	μ s
	Double speed operation ($V_{CC} = 3.0$ to 3.6 V)	0.125	—	1.0	μ s
	Quad speed operation	0.2	—	1.0	μ s
CPU is driven at the same clock rate as the external clock	Stopped or normal speed operation ($V_{CC} = 1.8$ to 3.0 V)	0.2	—	1.0	μ s
	Stopped or normal speed operation ($V_{CC} = 3.0$ to 3.6 V)	0.125	—	1.0	μ s
	Double speed operation ($V_{CC} = 1.8$ to 3.0 V)	0.2	—	1.0	μ s
	Double speed operation ($V_{CC} = 3.0$ to 3.6 V)	0.125	—	1.0	μ s
	Quad speed operation	0.2	—	1.0	μ s
CPU is driven by an external clock doubled by PLL	Stopped or normal speed operation ($V_{CC} = 1.8$ to 3.0 V)	0.2	—	1.0	μ s
	Stopped or normal speed operation ($V_{CC} = 3.0$ to 3.6 V)	0.125	—	1.0	μ s
	Double speed operation ($V_{CC} = 1.8$ to 3.0 V)	0.2	—	1.0	μ s
	Double speed operation ($V_{CC} = 3.0$ to 3.6 V)	0.125	—	1.0	μ s
	Quad speed operation	0.2	—	1.0	μ s
CPU is driven at the same clock rate as the external clock (doubled by PLL and then divided by 2)	Stopped or normal speed operation	0.2	—	1.0	μ s
	Double speed operation	0.2	—	1.0	μ s
	Quad speed operation	0.2	—	1.0	μ s

**Figure 4.1 CLK Input Waveform****Figure 4.2 System Clock Timing (Internal clock)**

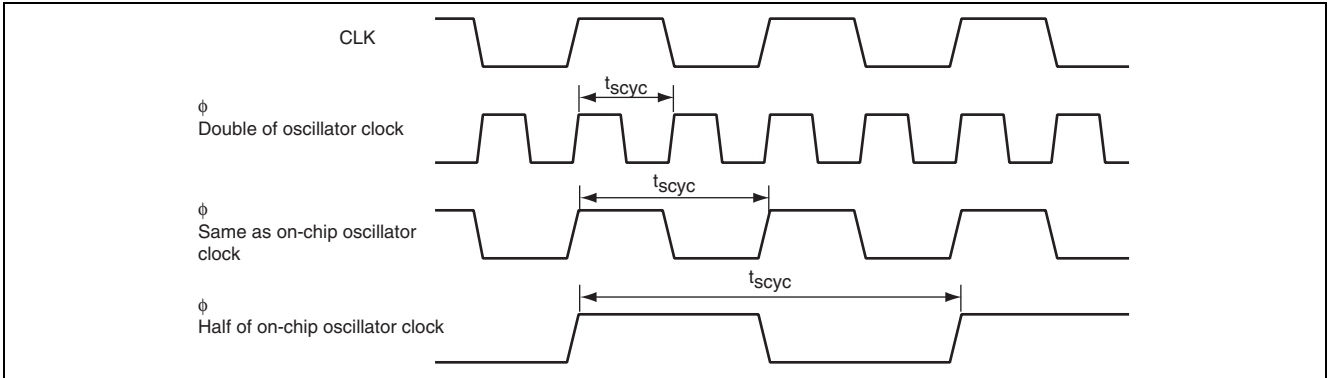


Figure 4.3 System Clock Timing (External clock)

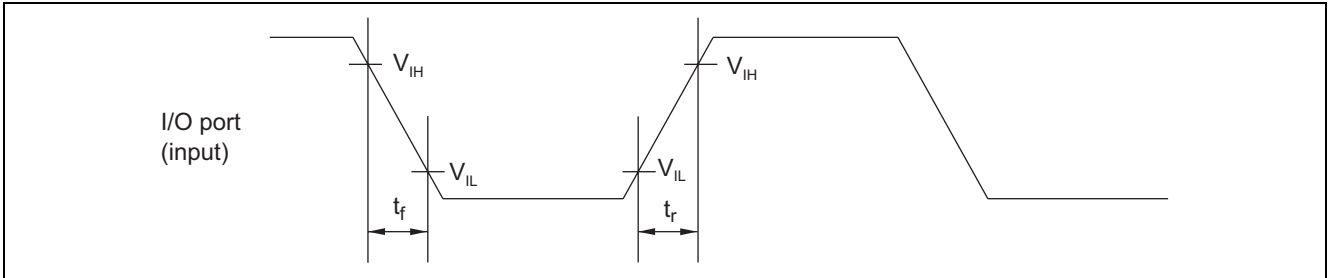


Figure 5 I/O Port Input Waveform

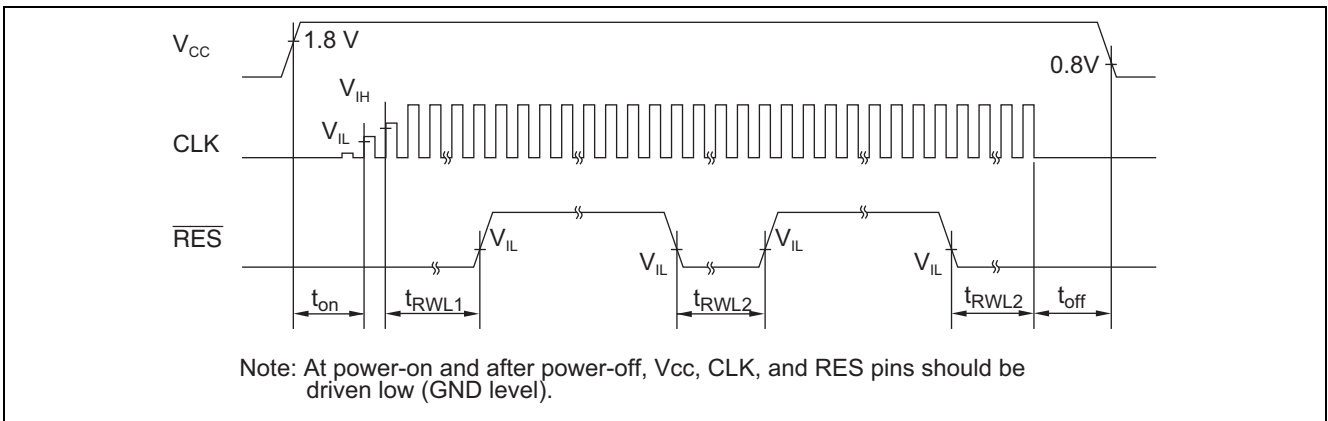


Figure 6 Power ON/OFF and \overline{RES} Input Timing

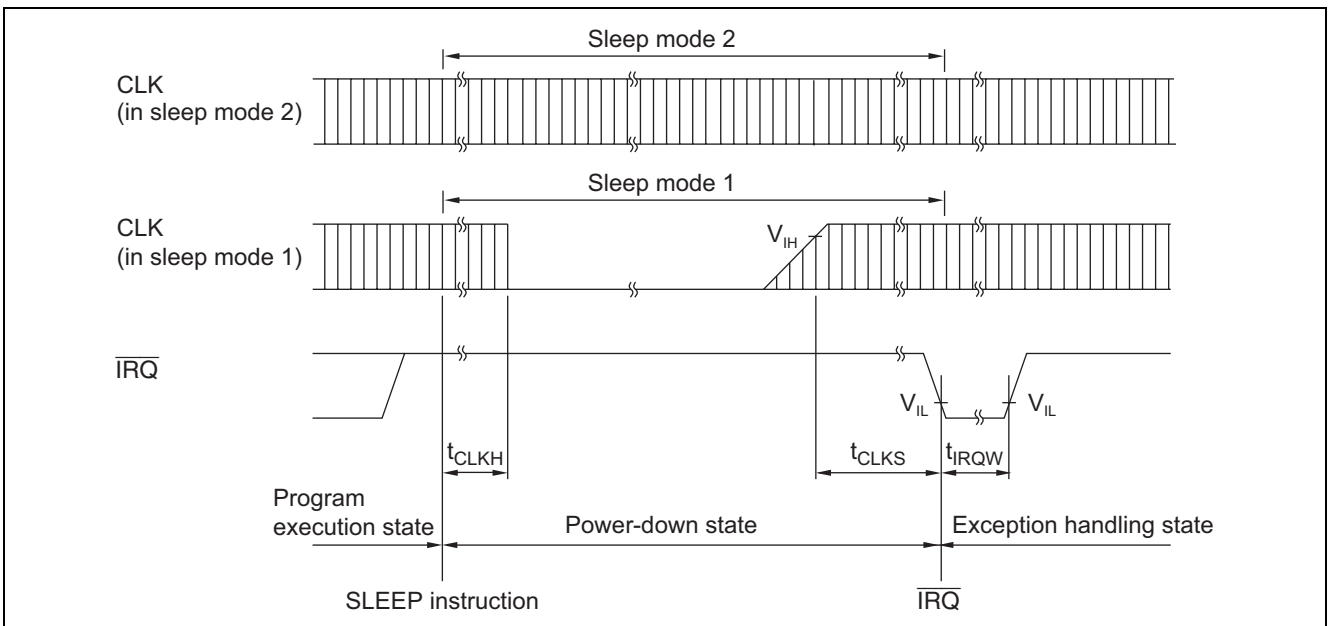


Figure 7 Interrupt Timing in Sleep Mode 1 and Sleep Mode 2

Reset Circuit Characteristics

Table 7 Reset Circuit Characteristics

Conditions: $V_{CC} = 1.8$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise specified.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power-on reset effective voltage	V_{POR1}	Figure 8	—	—	0.1	V
Power-on reset release voltage rise time	t_{PWON1}	Figure 8	—	—	0.5	ms
Power-on reset release voltage rise time	t_{PWON1}	Figure 8 $t_{POR1} \geq 1\text{s}^*$	—	—	1	ms
Power-on reset release time	t_{PRST}	Figure 8 $t_{POR1} \geq 10\text{s}^*$	—	—	500	μs

Note: * t_{POR1} is the time needed to enable the power-on reset by keeping the external power supply V_{CC} to lower than the effective voltage (V_{POR1}).

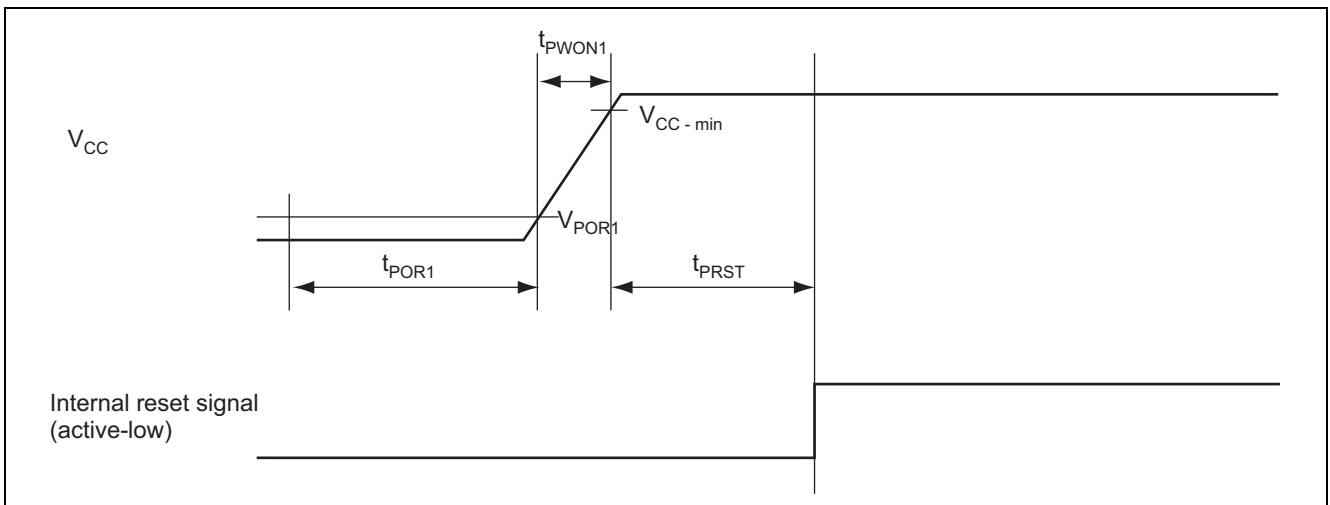


Figure 8 Power-On Reset Timing

Voltage Monitoring Circuit

Table 8 Voltage Monitoring Circuit Characteristics

Conditions: $V_{CC} = 1.8$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}$, unless otherwise specified.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Voltage detect level	V_{DET0}	Figure 9	1.9	2.3	2.6	V

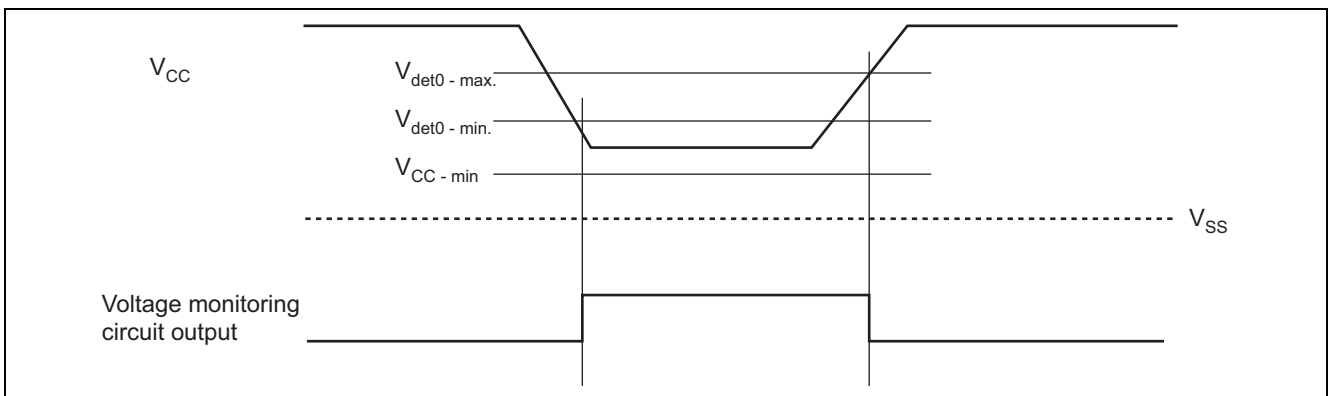


Figure 9 Voltage Monitoring Circuit Timing

Communication Interface Timing

Timing of Synchronous Communication Unit (SSU)

Table 9 Timing of Synchronous Communication Unit (SSU)

Conditions: $V_{CC} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_a = -20$ to $+75$ °C, $C_L = 30$ pF*, unless otherwise specified.

Item	Symbol	Applicable Pin	min.	typ.	max.	Unit	Test Conditions
Clock period	t_{SUCYC}	SCK	4	—	—	t_{scyc}	Figures 10 to figure 14
Clock high-level pulse width	t_{HI}	SCK	0.4	—	0.6	t_{SUCYC}	
Clock low-level pulse width	t_{LO}	SCK	0.4	—	0.6	t_{SUCYC}	
Clock rise time	Master	t_{RISE}	SCK	—	—	1	t_{scyc}
				Slave	—	—	0.1
Clock fall time	Master	t_{FALL}	SCK	—	—	1	t_{scyc}
				Slave	—	—	0.1
Data input setup time	t_{SU}	SSO, SSI	1	—	—	t_{scyc}	
Data input hold time	t_H	SSO, SSI	1	—	—	t_{scyc}	
\overline{CS} setup time	Slave	t_{LEAD}	\overline{CS}	4	—	—	t_{scyc}
\overline{CS} hold time	Slave	t_{LAG}	\overline{CS}	2	—	—	t_{scyc}
Data output delay time	t_{OD}	SSO, SSI	—	—	1	t_{scyc}	
Slave access time	t_{SA}	SSI	—	—	2	t_{scyc}	
Slave out release time	t_{OR}	SSI	—	—	2	t_{scyc}	

Note: * Load capacitance of the measured pins.

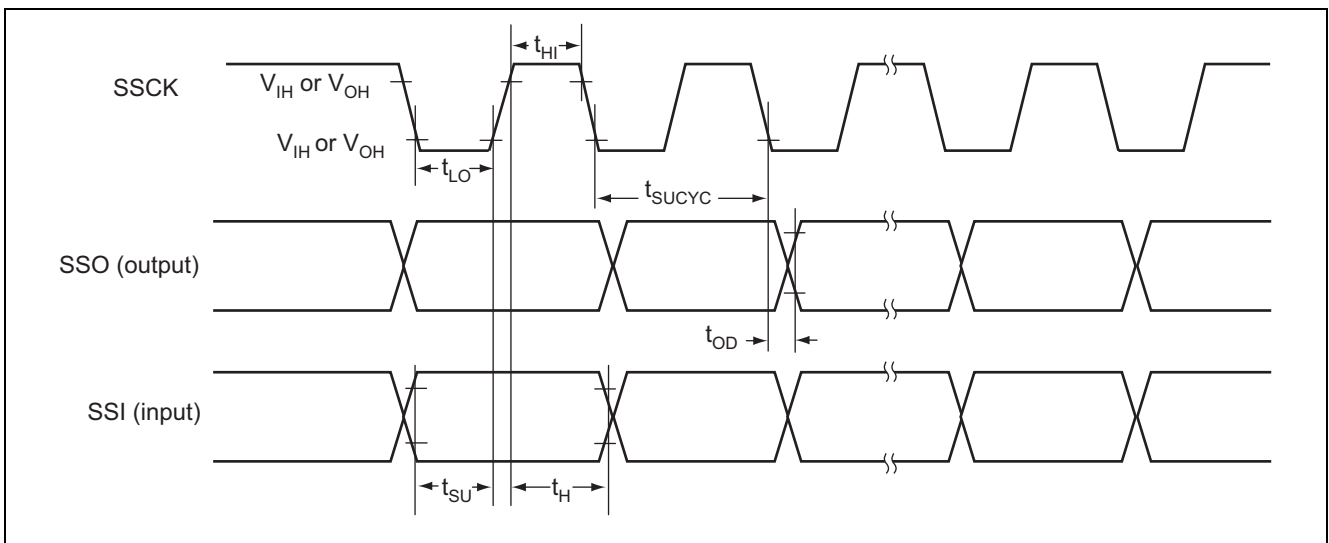


Figure 10 SSU I/O Timing (Clock Synchronous Mode)

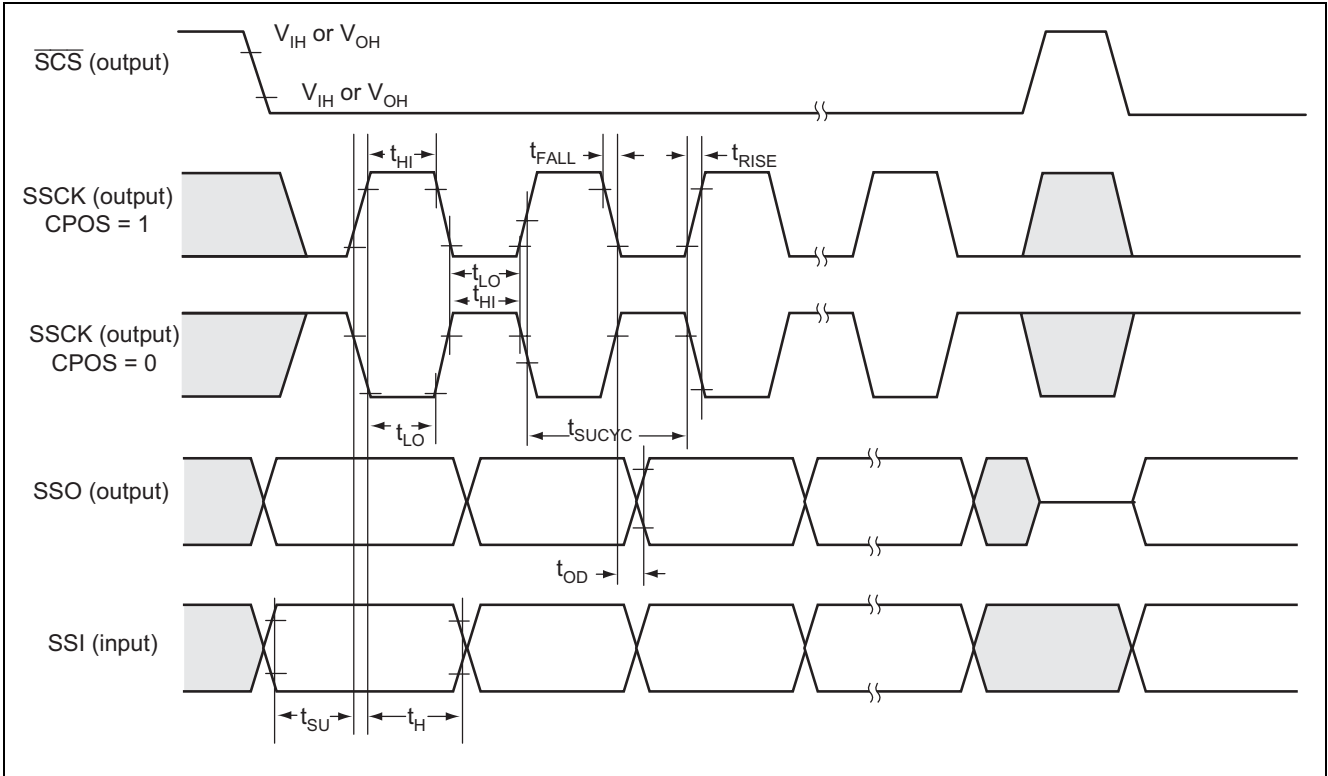


Figure 11 SSU I/O Timing (4-Line Bus Communication Mode, Master, CPHS = 1)

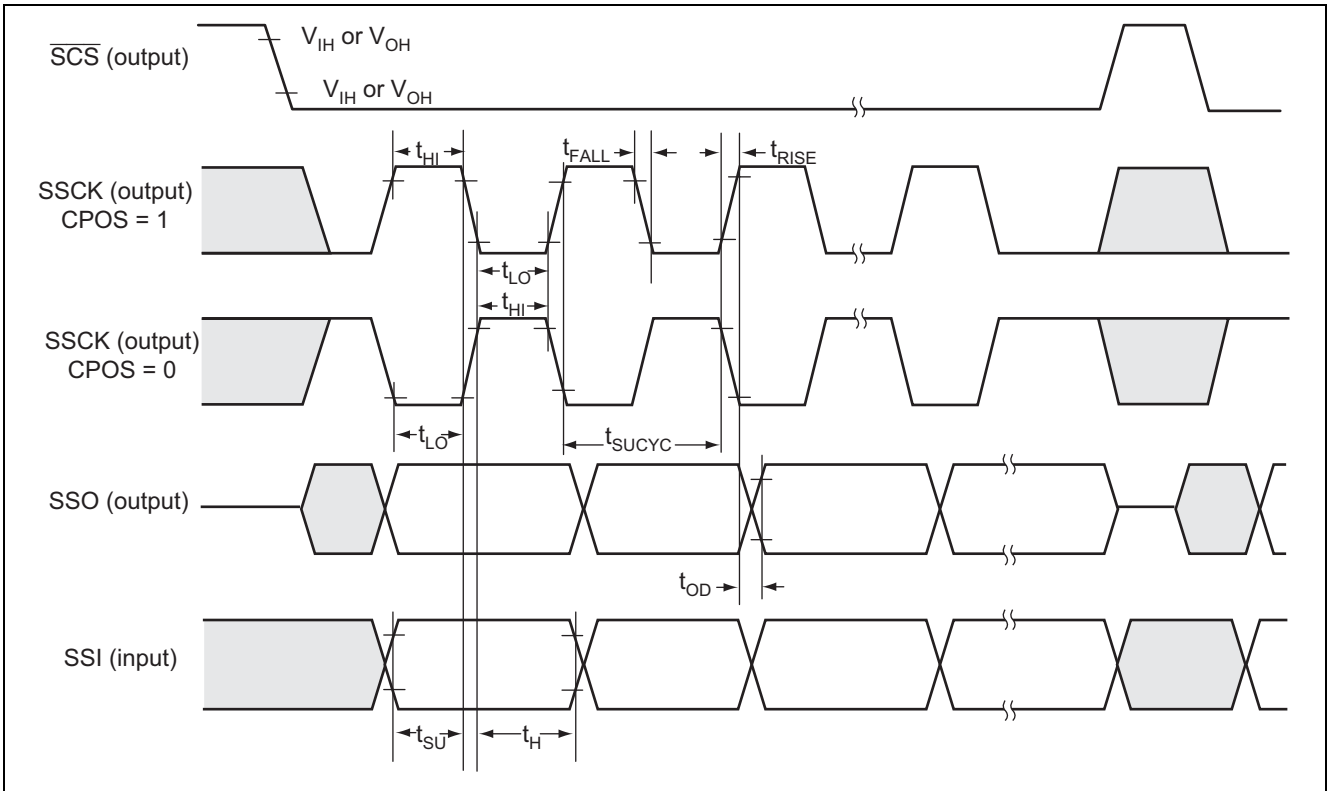


Figure 12 SSU I/O Timing (4-Line Bus Communication Mode, Master, CPHS = 0)

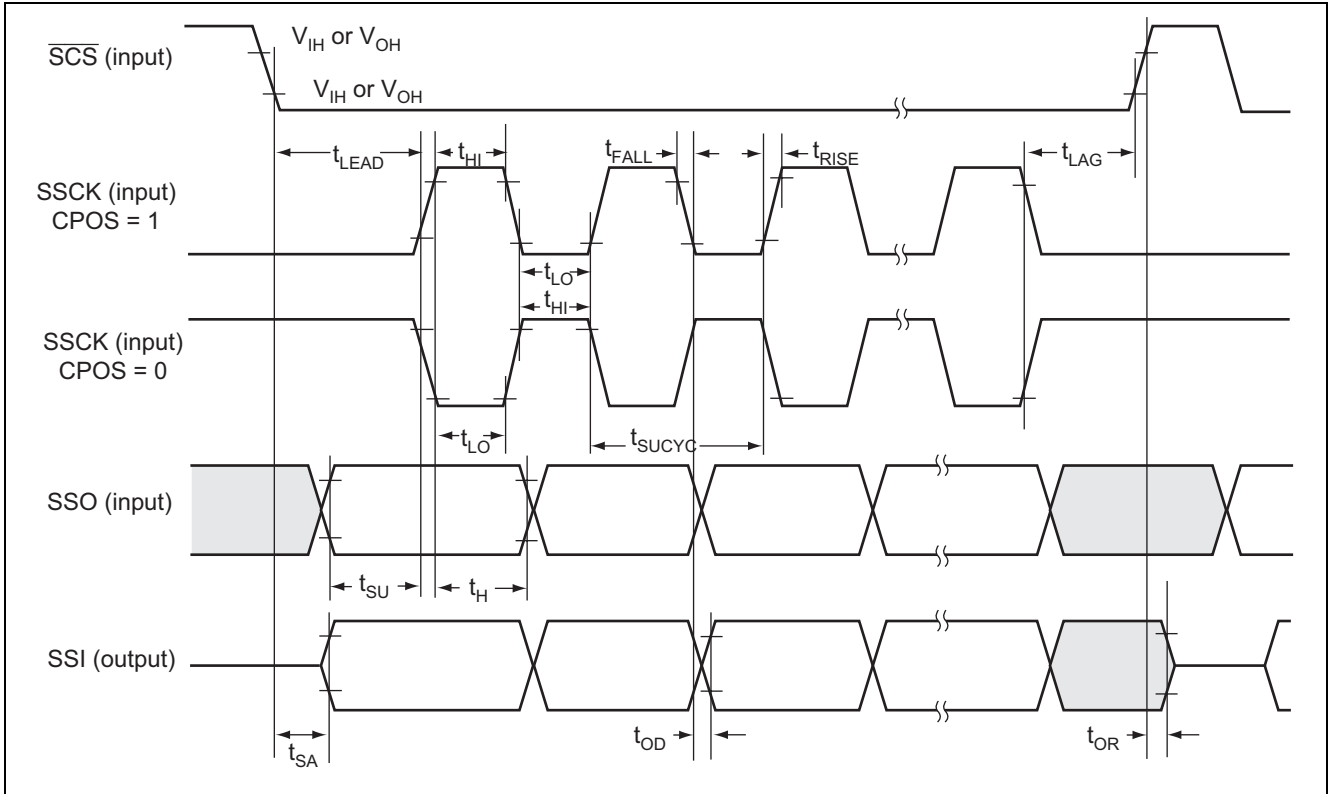


Figure 13 SSU I/O Timing (4-Line Bus Communication Mode, Slave, CPHS = 1)

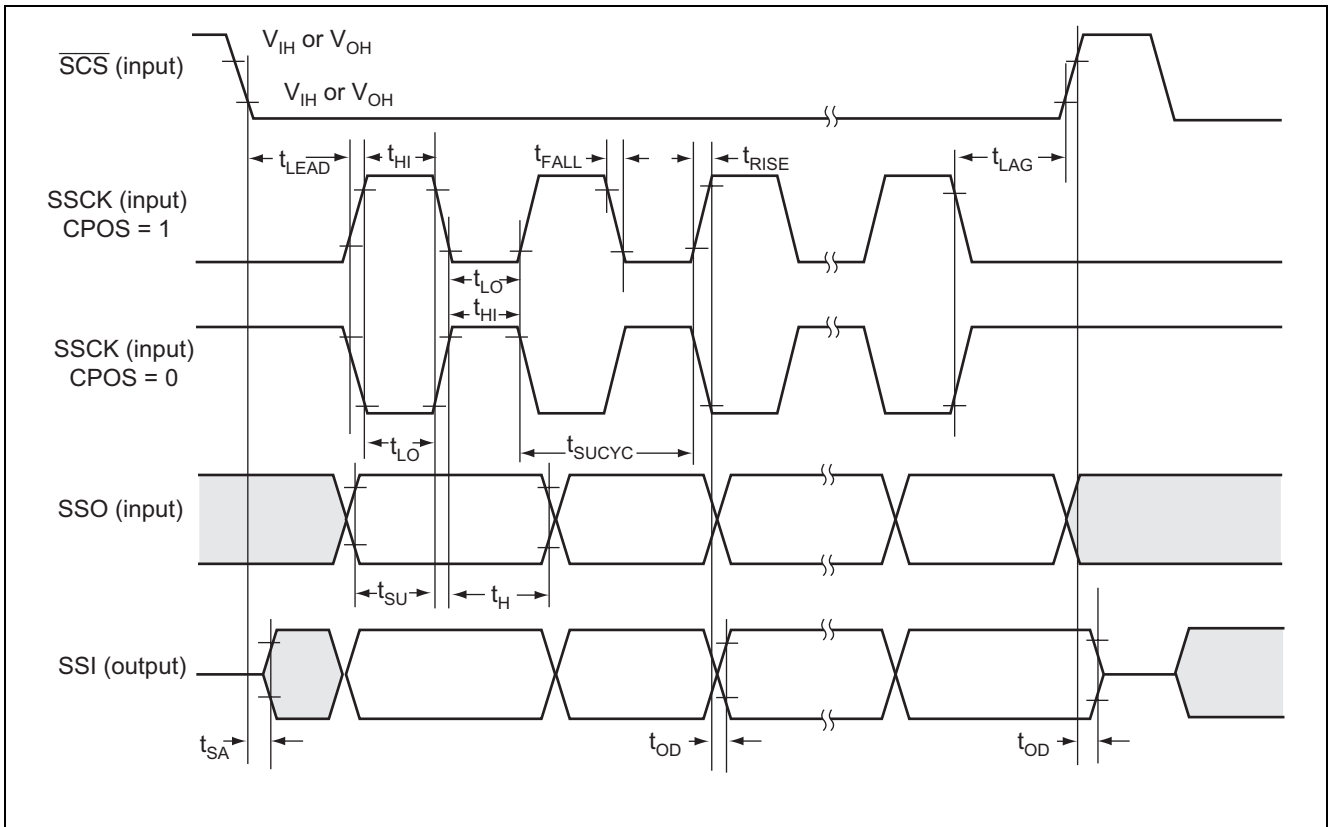


Figure 14 SSU I/O Timing (4-Line Bus Communication Mode, Slave, CPHS = 0)

Timing of I²C Bus Interface 2 (IIC2)

Table 10 Timing of I²C Bus Interface 2 (IIC2)

Conditions: V_{CC} = 3.0 to 3.6 V, V_{SS} = 0 V, T_a = -20 to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pin	min.	typ.	max.	Unit	Test Conditions
SCL input cycle time	t _{SCL}	SCL	12 t _{scyc} + 600	—	—	ns	Figures 15
SCL input high-level pulse width	t _{SCLH}	SCL	3 t _{scyc} + 300	—	—	ns	
SCL input low-level pulse width	t _{SCLL}	SCL	5 t _{scyc} + 300	—	—	ns	
SCL/SDA input fall time	t _{Sf}	SCL, SDA	—	—	300	ns	
SCL/SDA input spike pulse removal time	t _{SP}	SCL, SDA	—	—	1 t _{scyc}	t _{scyc}	
SDA input bus free time	t _{BUF}	SDA	5	—	—	t _{scyc}	
Start condition input hold time	t _{STAH}	SCL, SDA	3	—	—	t _{scyc}	
Repeated start condition input setup time	t _{STAS}	SCL, SDA	3	—	—	t _{scyc}	
Stop condition input setup time	t _{STOS}	SCL, SDA	3	—	—	t _{scyc}	
Data input setup time	t _{SDAS}	SDA	1 t _{scyc} + 20	—	—	ns	
Data input hold time	t _{SDAH}	SDA	0	—	—	ns	

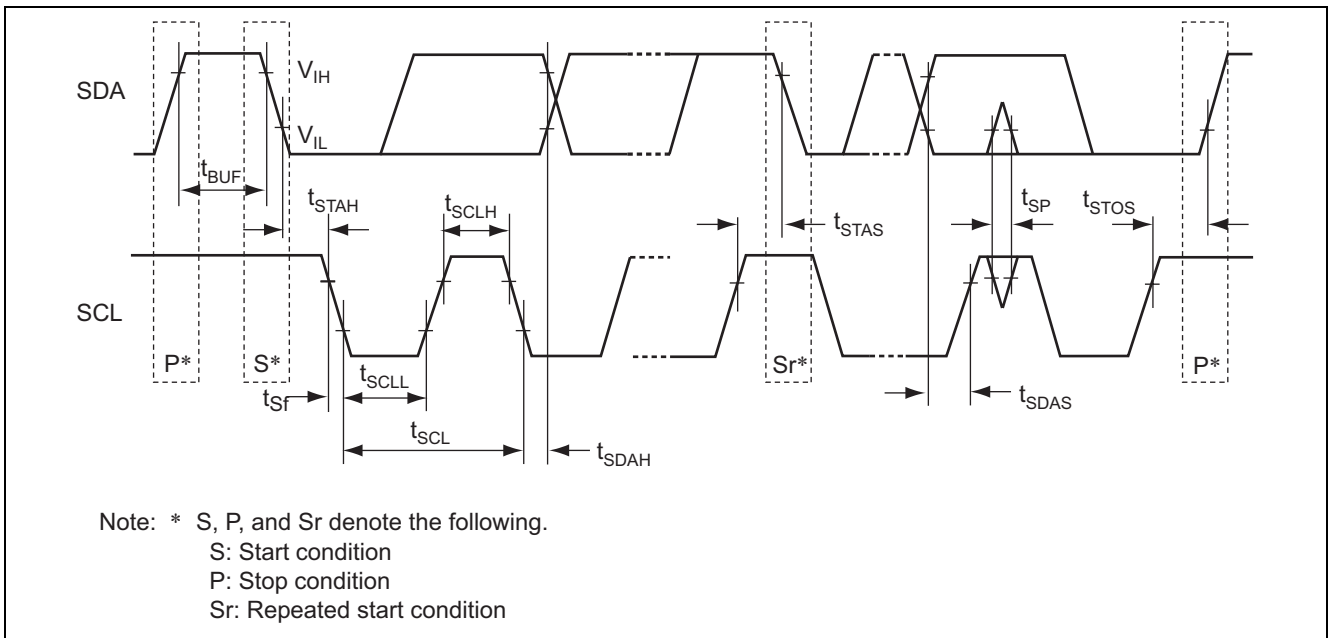


Figure 15 I/O Timing of I²C Bus Interface 2

Revision History

R5H30211 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2008.Jul.29	—	First edition issued
1.10	2009.Jun.05	1	A logo mark is added to the cover page.
		5	Figure 2 The pin number (pin 13) in the pin assignment figure was changed.
		9	Table 5 The minimum values of the items " $\overline{\text{RES}}$ pulse width" and "interrupt pulse width (IRQ)" were changed. "A system clock (f) cycle time (external clock)" were added. Part of the symbols and units were changed from t_{cyc} to t_{scyc} . Reference figures were changed because figures 4.2 and 4.3 were added.
		10	Table 6 The item of "the CPU operates on the clock pulse obtained by multiplying the external clock frequency by two using the internal PLL" was changed.
		10 to 11	The figure number of figure 4 was changed to figure 4.1. Figures 4.2 and 4.3 were added.
		13	Table 9 The item of "min, typ, and max" was changed. The unit of t_{cyc} was changed to t_{scyc} .
		16	Table 10 The item of "min, typ, and max" were changed. The unit of t_{cyc} was changed to t_{scyc} .

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510